Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-3. (Cancelled)

4. (Currently Amended) The display of claim 17, wherein in order to install said control circuit in a control circuit accommodation portion of said ~~first~~ TFT substrate, said control circuit accommodation portion is made thinner than other portions of said ~~first~~ TFT substrate.

5. (Cancelled)

6. (Currently Amended) The display of claim 17, wherein said control circuit is packed over said ~~first~~ TFT substrate by COG (chip-on-glass) technology.

7-12. (Cancelled)

13. (Previously Presented) The method of claim 24, further comprising the step of thinning a portion of said counter substrate which is located opposite to a control circuit for controlling said driver circuit made up of said driver TFTs, to install said control circuit.

14. (Currently Amended) The method of claim 24, wherein said control circuit is packed over said ~~first~~ TFT substrate by COG (chip-on-glass) technology.

15-16. (Cancelled)

17. (Currently Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a ~~first~~ TFT substrate and arrayed in a matrix;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a layer of a liquid crystal material provided between said ~~first~~ TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said ~~first~~ TFT substrate and said counter substrate;

a driver TFT provided over said ~~first~~ TFT substrate; and

a control circuit comprising a control circuit chip ~~provided under and in contact with~~ sealed in said sealing material, said control circuit provided over said ~~first~~ TFT substrate for controlling said driver TFT.

18-20. (Cancelled)

21. (Currently Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a ~~first~~ TFT substrate and arrayed in a matrix;

a bus line provided over said ~~first~~ TFT substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a layer of a liquid crystal material provided between said ~~first~~ TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said ~~first~~ TFT substrate and said counter substrate;

a driver TFT provided over said ~~first~~ TFT substrate; and

a control circuit comprising a control circuit chip ~~provided under and in contact with~~ sealed in said sealing material, said control circuit provided over said ~~first~~ TFT substrate for controlling said driver TFT.

22. (Currently Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a ~~first~~ TFT substrate and arrayed in a matrix;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a layer of a liquid crystal material provided between said ~~first~~ TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said ~~first~~ TFT substrate and said counter substrate, said sealing material being provided outside at least said pixel TFTs;

a driver TFT provided over said ~~first~~ TFT substrate; and

a control circuit comprising a control circuit chip ~~provided under and in contact with~~ sealed in said sealing material, said control circuit provided over said ~~first~~ TFT substrate for controlling said driver TFT.

23. (Currently Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a ~~first~~ TFT substrate and arrayed in a matrix;

a bus line provided over said ~~first~~ TFT substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a layer of a liquid crystal material provided between said ~~first~~ TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said ~~first~~ TFT substrate and said counter substrate, said sealing material being provided outside at least said pixel TFTs;

a driver TFT provided over said ~~first~~ TFT substrate; and

a control circuit comprising a control circuit chip ~~provided under and in contact with~~ sealed in said sealing material, said control circuit provided over said ~~first~~ TFT substrate for controlling said driver TFT.

24. (Currently Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a ~~first~~ TFT substrate and arrayed in a matrix;

a bus line provided over said ~~first~~ TFT substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a layer of a liquid crystal material provided between said ~~first~~ TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said ~~first~~ TFT substrate and said counter substrate and outside at least said pixel TFTs;

a driver TFT provided over said ~~first~~ TFT substrate; and

a control circuit comprising a control circuit chip ~~provided under and in contact with~~ sealed in said sealing material, said control circuit provided over said ~~first~~ TFT substrate for controlling said driver TFT,

said method comprising:

cutting said ~~first~~ TFT substrate and said counter substrate outside said sealing material having said control circuit ~~under and in contact with~~ sealed in said sealing material.

25. (Currently Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a ~~first~~ TFT substrate and arrayed in a matrix;

a bus line provided over said ~~first~~ TFT substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a layer of a liquid crystal material provided between said ~~first~~ TFT substrate and said counter substrate;

a sealing material sealing around said liquid crystal material and provided between said ~~first~~ TFT substrate and said counter substrate;

a driver TFT provided over said ~~first~~ TFT substrate; and

a control circuit comprising a control circuit chip ~~provided under and in contact with~~ sealed in said sealing material, said control circuit provided over said ~~first~~ TFT substrate for controlling said driver TFT,

said method comprising:

cutting said ~~first~~ TFT substrate and said counter substrate outside said sealing material having said control circuit ~~under and in contact with~~ sealed in said sealing material.

26-29. (Cancelled)

30. (Currently Amended) The display of claim 21, wherein in order to install said control circuit in a control circuit accommodation portion of said ~~first~~ TFT substrate, said counter substrate has a thinned portion located opposite to said control circuit accommodation portion.

31. (Currently Amended) The display of claim 21, wherein said control circuit is packed over said ~~first~~ TFT substrate by COG (chip-on-glass) technology.

32-34. (Cancelled)

35. (Currently Amended) The display of claim 22, wherein in order to install said control circuit in a control circuit accommodation portion of said ~~first~~ TFT substrate, said counter substrate has a thinned portion located opposite to said control circuit accommodation portion.

36. (Currently Amended) The display of claim 22, wherein said control circuit is packed over said ~~first~~ TFT substrate by COG (chip-on-glass) technology.

37-39. (Cancelled)

40. (Currently Amended) The display of claim 23, wherein in order to install said control circuit in a control circuit accommodation portion of said ~~first~~ TFT substrate, said counter substrate has a thinned portion located opposite to said control circuit accommodation portion.

41. (Currently Amended) The display of claim 23, wherein said control circuit is packed over said ~~first~~ TFT substrate by COG (chip-on-glass) technology.

42. (Previously Presented) The method of claim 25, wherein said cutting step is carried out in such a way that said cut side edges to which said nonconductive or weakly conductive material is applied or adhesively bonded are parallel or vertical to a direction of array of said pixel TFTs.

43. (Cancelled)

44. (Previously Presented) The method of claim 25, further comprising the step of thinning a portion of said counter substrate which is located opposite to said control circuit, to install said control circuit.

45-60. (Cancelled)

61. (Currently Amended) A semiconductor device including at least one liquid crystal panel having at least a first side, a second side, a third side, and a fourth side, said liquid crystal panel comprising:

a TFT substrate comprising a glass;

a pixel TFT provided over ~~a first~~ said TFT substrate ~~comprising a glass~~;

a channel formation region provided in a semiconductor film provided over said ~~first~~ TFT substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a bus line provided over said ~~first~~ TFT substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said ~~first~~ TFT substrate;

a sealing material provided between said ~~first~~ TFT substrate and said counter substrate; and

a nonconductive material applied to ~~a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line, said nonconductive material applied to three sides of said first substrate and three sides of said counter substrate~~ the first side, the second side, and the third side of said liquid crystal panel,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said nonconductive material is not applied to ~~one side of said first substrate and is not applied to one side of said counter substrate~~ the fourth side of said liquid crystal panel.

62. (Currently Amended) A semiconductor device including at least one liquid crystal panel having at least a first side, a second side, a third side, and a fourth side, said liquid crystal panel comprising:

a TFT substrate comprising a glass;

a pixel TFT provided over ~~a first~~ said TFT substrate ~~comprising a glass~~;

a channel formation region provided in a semiconductor film provided over said ~~first~~ TFT substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a bus line provided over said ~~first~~ TFT substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said ~~first~~ TFT substrate;

a sealing material provided between said ~~first~~ TFT substrate and said counter substrate; and

a weakly conductive material applied to ~~a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line, said weakly conductive material applied to three sides of said first substrate and three sides of said counter substrate~~ the first side, the second side, and the third side of said liquid crystal panel,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said weakly conductive material is not applied to ~~one side of said first substrate and is not applied to one side of said counter substrate~~ the fourth side of said liquid crystal panel.

63. (Currently Amended) A semiconductor device including at least one liquid crystal panel having at least a first side, a second side, a third side, and a fourth side, said liquid crystal panel comprising:

a TFT substrate comprising a glass;

a pixel TFT provided over a ~~first~~ TFT substrate ~~comprising a glass~~;

a channel formation region provided in a semiconductor film provided over said ~~first~~ TFT substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a driver TFT provided over said ~~first~~ TFT substrate;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a bus line provided over said ~~first~~ TFT substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said ~~first~~ TFT substrate;

a sealing material provided between said ~~first~~ TFT substrate and said counter substrate; and

a nonconductive material applied to ~~a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line, said weakly conductive material applied to three sides of said first substrate and three sides of said counter substrate~~ the first side, the second side, and the third side of said liquid crystal panel,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said nonconductive material is not applied to ~~one the other side of said first substrate and is not applied to one side of said counter substrate~~ the fourth side of said liquid crystal panel.

64. (Currently Amended) A semiconductor device including at least one liquid crystal panel having at least a first side, a second side, a third side, and a fourth side, said liquid crystal panel comprising:

a TFT substrate comprising a glass;

a pixel TFT provided over a ~~first~~ TFT substrate ~~comprising a glass~~;

a channel formation region provided in a semiconductor film provided over said ~~first~~ TFT substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, said pixel TFT comprising said channel formation region and said gate electrode and said gate insulating film;

a driver TFT provided over said ~~first~~ TFT substrate;

a counter substrate located opposite to said ~~first~~ TFT substrate;

a bus line provided over said ~~first~~ TFT substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said ~~first~~ TFT substrate;

a sealing material provided between said ~~first~~ TFT substrate and said counter substrate; and

a weakly conductive material applied to ~~a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line, said weakly conductive material applied to three sides of said first substrate and three sides of said counter substrate~~ the first side, the second side, and the third side of said liquid crystal panel,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said weakly conductive material is not applied to ~~one side of said first substrate and is not applied to one side of said counter substrate~~ the fourth side of said liquid crystal panel.

65-68. (Cancelled)

69. (Currently Amended) The display of claim 61 wherein said part of said bus line is aligned with said ~~side edge of said counter substrate and said~~ side edge of said ~~first~~ TFT substrate.

70. (Currently Amended) The display of claim 62 wherein said part of said bus line is aligned with said ~~side edge of said counter substrate and said~~ side edge of said ~~first~~ TFT substrate.

71. (Currently Amended) The display of claim 63 wherein said part of said bus line is aligned with said ~~side edge of said counter substrate and said~~ side edge of said ~~first~~ TFT substrate.

72. (Currently Amended) The display of claim 64 wherein said part of said bus line is aligned with said ~~side edge of said counter substrate and said~~ side edge of said ~~first~~ TFT substrate.